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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,463	11/05/2003	Takahiro Senda	1035-478	6395

23117 7590 11/15/2006

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EXAMINER	
KUMAR, SRILAKSHMI K	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,463	SENDA ET AL.	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *2,4,6,8 and 10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,7 and 9-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/2003 & 6/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The following office action is in response to the Election Response filed on August 1, 2006. Claims 1-14 are pending, with Applicant electing claims of Species I, Claims 1, 3, 5, 7 and 9-14.

Election/Restrictions

Applicant has elected claims of Species I without traverse. The following claims are included in Species I: 1, 3, 5, 7, 9-14.

Drawings

1. Figures 13-16 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kasai (US PG-PUB 2003/003060).

As to **independent claim 1**, Kasai discloses a display device (Fig. 2), setting a value of a current allowed to flow to an electro-optic element of each pixel so as to drive the electro optic element on the basis of current (page 3, paragraph 0063, where it is taught that the pixel circuit is a current-program type circuit that adjusts the emission level of the organic EL element in accordance with the current value), wherein the pixel (Fig. 4, item 210) includes; a first wiring (Fig. 4, Vdd, is the power wiring) for allowing the current to flow to the electro optic element (Fig. 4, item 220 is the EL element; and page 3, paragraph 0064 where the power supply is connected);

Kasai discloses a first active element (Fig. 4, item 214), provided in series to the electro-optic element (Fig 4, item 220) so as to be positioned in a path for allowing the current to flow from the first wiring to the electro optic element (shown in Fig. 4, where the current flow is from Vdd and item 214 which is the first active element is in the path of the electro optic element, item 220), which has a control terminal for controlling conductance of the first active element (the control terminal shown by the gate of 214, and page 3, paragraph 0067);

Kasai discloses a second active element (Fig. 4, item 213), provided in series to the electro optic element and the first active element so as to be positioned in the path (Fig. 4, item 213 is shown to be between the electro optic element, item 220 and the first active element, item 214), which has a control terminal for allowing/disallowing conduction (shown by the gate which is connected to V2);

Kasai discloses an electric charge retaining section (Fig. 4, item 230, the capacitor) for storing electric charge so as to apply a voltage corresponding to thus stored electric charge to the control terminal of the first active element as a control voltage for controlling the conductance of

the first active element (page 3, paragraph 0063, and page 4, paragraph 0072; where the capacitor corresponds to a voltage holding means which is then applied to the first active element);

Kasai discloses a third active element (Fig. 4, item 211), provided in a path for supplying the electric charge to the electric charge retaining section (page 3, paragraph 0067 where the third active element is used to supply electric charge), which has a control terminal for allowing/disallowing conduction (Fig. 4, shown by the gate which is connected to V1), said third active element causing the electric charge retaining section to retain the electric charge by disallowing conduction (page 4, paragraph 0073, where the gate signal V1 is set to an L level or low level, thus switches the third active element to the off state);

Kasai discloses a second wiring (Fig. 4, item V2) for applying a control voltage for allowing/disallowing conduction to the control terminal of the second active element (page 4, paragraph 0074); and

Kasai discloses a third wiring (Fig. 4, item V1) for applying a control voltage for allowing/disallowing conduction to the control terminal of the third active element (page 4, paragraphs 0071, 0073 and 0074, wherein V1 is set to high in order to allow conduction to the third active element, and V1 is set to low in order to disallow conduction to the third active element).

As to **independent claim 9**, Kasai discloses a display device (Fig. 2), setting a value of a current allowed to flow to an electro optic element of each pixel so as to drive the electro optic element on the basis of the current (page 3, paragraph 0063, where it is taught that the pixel

circuit is a current-program type circuit that adjusts the emission level of the organic EL element in accordance with the current value), wherein the first pixel (Fig. 4, item 210) includes:

Kasai discloses a firstly ordered (Fig. 4, Vdd, is the power wiring) wiring for allowing the current to flow to the electro optic element (Fig. 4, item 220 is the EL element; and page 3, paragraph 0064 where the power supply is connected);

Kasai discloses a firstly ordered active element (Fig. 4, item 214), provided in series to the electro optic element (Fig 4, item 220) so as to be positioned in a path for allowing the current to flow from the firstly ordered wiring to the electro optic element (shown in Fig. 4, where the current flow is from Vdd and item 214 which is the first active element is in the path of the electro optic element, item 220), which has a control terminal for controlling conduction of the firstly ordered active element (the control terminal shown by the gate of 214, and page 3, paragraph 0067);

Kasai discloses an electric charge retaining section (Fig. 4, item 230, the capacitor) for storing electric charge so as to apply a voltage corresponding to thus stored electric charge to the control terminal of the firstly ordered active element as a control voltage for controlling the conductance of the firstly ordered active element (page 3, paragraph 0063, and page 4, paragraph 0072; where the capacitor corresponds to a voltage holding means which is then applied to the first active element);

Kasai discloses a secondly ordered active element (Fig. 4, item 211), provided in a path for supplying the electric charge to the electric charge retaining section (page 3, paragraph 0067 where the active element is used to supply electric charge), which has a control terminal for allowing/disallowing conduction (Fig. 4, shown by the gate which is connected to V1), said

secondly ordered active element causing the electric charge retaining section to retain the electric charge by disallowing conduction (page 4, paragraph 0073, where the gate signal V1 is set to an L level or low level, thus switches the active element to the off state);

Kasai discloses a secondly ordered wiring (Fig. 4, item V2) for applying a control voltage for allowing/disallowing conduction to the control terminal of the secondly-ordered active element (page 4, paragraph 0074); and

Kasai discloses a thirdly ordered wiring (Fig. 4, item V1) for providing a reference voltage, which is a fraction of the voltage corresponding to the electric charge stored in the electric charge retaining section (page 4, paragraphs 0071, 0073 and 0074).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 3, 5, 7, and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai (US PG-PUB 2003/003060) in view of Bae et al (US PG-PUB 2002/0075208).

As to **independent claim 13**, Kasai discloses a display device (Fig. 2), setting a value of a current allowed to flow to an electro-optic element of each pixel so as to drive the electro optic element on the basis of the current, wherein the pixel includes:

Kasai discloses a wiring (Fig. 4, item Vdd) for allowing the current to flow to the electro optic element (Fig. 4, item 220 is the EL element, where the current flows through Vdd into 220);

Kasai discloses an active element (Fig. 4, item 213), provided in series to the electro optic element so as to be positioned in a path for allowing the current to flow from the wiring to the electro optic element (Fig. 4, where item 213 is shown to be in series with the electro optic element 220), which has a control terminal for controlling conductance of the active element (the control terminal shown by the gate of 214, and page 3, paragraph 0067); and

Kasai discloses an electric charge retaining section (Fig. 4, item 230, the capacitor) for storing electric charge so as to apply a voltage corresponding to thus stored electric charge to the control terminal of the active element as a control voltage for controlling the conductance of the active element (page 3, paragraph 0063, and page 4, paragraph 0072; where the capacitor corresponds to a voltage holding means which is then applied to the active element).

Kasai does not explicitly teach where the display device includes a current source circuit which outputs a constant current to the wiring so as to perform a first operation in which the electric charge retaining section is made to store electric charge corresponding to the current which has been allowed to flow to the active element so that a circuit of the pixel memorizes the

current; and a voltage source circuit which outputs a low voltage so as to perform a second operation, in which the current memorized in the circuit is allowed to flow to the electro optic element via the active element, after performing the first operation, said current source circuit and said voltage source circuit being provided in a switchable manner.

Bae et al teach where a display device includes a current source circuit (Fig. 5, shown by item II which is a current mirror) which outputs a constant current to the wiring so as to perform a first operation in which the electric charge retaining section is made to store electric charge corresponding to the current which has been allowed to flow to the active element so that a circuit of the pixel memorizes the current (Page 3, paragraphs 0060-0062, where in the third embodiment, constant currents are output so as to store charge and allow current to flow to the active element). Bae et al teach where a voltage source circuit which outputs a low voltage so as to perform a second operation in which the current memorized in the circuit is allowed to flow to the electro optic element via the active element, after performing the first operation, said current source circuit and said voltage source circuit are being provided in a switchable manner (Page 3, paragraphs 0064-0068).

It would have been obvious to one of ordinary skill in the art to include the current mirror as taught by Bae et al into the display device of Kasai because, by doing so, the current mirror of Bae et al enables a driving circuit that can control an output current value according to red, green and blue channels by receiving a digital signal of n bits, thereby improving packing density of an integrated circuit for driving current.

As to **dependent claim 3**, limitations of claim 1, and further comprising, Kasai does not teach wherein a current source circuit and a voltage source circuit are connected to the first

wiring in a switchable manner. Bae et al teaches wherein a current source circuit (Fig. 5) and a voltage source circuit (Fig. 5) are connected to the first wiring in a switchable manner (Fig. 5 Iref and Isink). It would have been obvious to one of ordinary skill in the art to include the current mirror as taught by Bae et al into the display device of Kasai because, by doing so, the current mirror of Bae et al enables a driving circuit that can control an output current value according to red, green and blue channels by receiving a digital signal of n bits, thereby improving packing density of an integrated circuit for driving current.

As to **dependent claim 5**, limitations of claim 3, and further comprising, Bae et al disclose wherein a first operation is performed, and a second operation is performed thereafter, said first operation being such that: the current source is connected to the first wiring so as to set the value of the current allowed to flow to the electro optic element of the pixel (Page 3, paragraphs 0060-0062), said second operation being such that; the voltage source circuit is connected to the first wiring so as to allow the current whose value has been set by performing the first operation to flow to the electro optic element of the pixel (Page 3, paragraphs 0064-0068).

As to **dependent claim 7**, limitations of claim 5, and further comprising, Bae et al disclose wherein the current source circuit outputs a plurality of current values, and the first operation and the second operation that is performed after the first operation are performed plural at times at a predetermined period (Page 3, paragraphs 0060-0062, for RGB).

As to **dependent claim 10**, limitations of claim 9, and further comprising, Kasai does not teach wherein a current source circuit and a voltage source circuit are connected to the first wiring in a switchable manner. Bae et al teaches wherein a current source circuit (Fig. 5) and a

voltage source circuit (Fig. 5) are connected to the first wiring in a switchable manner (Fig. 5 Iref and Isink). It would have been obvious to one of ordinary skill in the art to include the current mirror as taught by Bae et al into the display device of Kasai because, by doing so, the current mirror of Bae et al enables a driving circuit that can control an output current value according to red, green and blue channels by receiving a digital signal of n bits, thereby improving packing density of an integrated circuit for driving current.

As to **dependent claim 11**, limitations of claim 10, and further comprising, Bae et al disclose wherein a first operation is performed, and a second operation is performed thereafter, said first operation being such that: the current source is connected to the first wiring so as to set the value of the current allowed to flow to the electro optic element of the pixel (Page 3, paragraphs 0060-0062), said second operation being such that; the voltage source circuit is connected to the first wiring so as to allow the current whose value has been set by performing the first operation to flow to the electro optic element of the pixel (Page 3, paragraphs 0064-0068).

As to **dependent claim 12**, limitations of claim 11, and further comprising, Bae et al disclose wherein the current source circuit outputs a plurality of current values, and the first operation and the second operation that is performed after the first operation are performed plural at times at a predetermined period (Page 3, paragraphs 0060-0062, for RGB).

As to **dependent claim 14**, limitations of claim 13, and further comprising, Bae et al disclose wherein the current source circuit outputs a plurality of current values, and the first operation and the second operation that is performed after the first operation are performed plural at times at a predetermined period (Page 3, paragraphs 0060-0062, for RGB).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 571 272 7769. The examiner can normally be reached on 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571 272 3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Srilakshmi K. Kumar
Examiner
Art Unit 2629

SKK
November 13, 2006